The Examiner's contentions with respect to the restriction requirement is again traversed, as is the Examiner's contention that there is no "generic" claim. The Examiner's attention is directed to claim 13 (with structures labeled with numbers from Figures 3, 5, 7 & 8) which is reproduced below:

> A direct memory access controller (40) for controlling data transfer between a data source (10) and a data destination (20) comprising:
>
> a single read/write port (47) comprising a read channel (47a) operable to receive data from said data source via a read path (33) on a bus (32) and a write channel (47c) operable to output said received data to said data destination (20) via a write path (35) on said bus (32), said read and write channel being operable to perform data reads and writes independently of each other.

By reviewing the above independent claim 13 and Figures 3, 5, 7 and 8 in Applicants' specification, it will be seen that every element and every recited interrelationship in claim 13 is disclosed in each of Figures 3, 5, 7 and 8. While there are differences between the figures, those differences are not recited in Claim 13 and therefore claim 13 must be considered generic to the alleged different species in the four figures.

While the Examiner contends that the existence of a register bank, whether or not a register bank exists in the figures, requires that the figures relate to different species, it is clear that claim 13, not claiming a specific "register bank," is not limited to any one figure and therefore is generic to all four figures. Thus, it is respectfully requested that the Examiner, as a minimum, confirm that claim 13 is a generic claim and, if allowable, will result in the examination of a reasonable number of species, i.e., those disclosed in Applicants' figures, i.e., Species I-III disclosed in Figures 3, 5, 7 and 8.

Claims 13-16 and 28-31 stand rejected under 35 USC §102(e) as being anticipated by Minami (U.S. Patent 6,651,114). It is noted that both independent claims 13 and 28 specify that the claimed read channel and write channel performs "data reads and writes independently of each other." The Examiner alleges that the structure of claims 13 and 28 are disclosed at column 1, lines 23-26 of the Minami reference (see the first parenthetical expression in bold on page 5 of the Official Action quoting from the Minami reference). Applicants agree that the Examiner has correctly recited column 1, lines 22-26, but would point out that this portion of Minami does not state or infer that the read and write channel are operable "to perform data reads and writes independently of each other."

Moreover, Applicants' independent claims 13 & 28 require a **single read/write port** which has both a read channel and a write channel and that these two channels can operate and perform data reads and writes **independently of each other**. In each of the two recited functions in the Minami reference, two completely different ports are required.

For the recited first function in Minami, the DMA controller 280 communicates with the I/O bus 270 through the port connecting I/O bus 270 with DMA controller 280 (the "I/O Bus Port") and "writes the data into the main storage" (RAM 220) by means of the system bus port connecting the DMA controller 280 to the system bus 200 (the "System Bus Port"). Thus, for the first function, an I/O Bus Port and a System Bus Port are required to output data from the I/O devices 240, 250 and 260 to the main storage 220.

Similarly, in the recited other function, the DMA controller 280 reads data out from the main storage 220 by means of the System Bus Port connecting the DMA controller to the system

bus and passes that data to the I/O devices by means of the I/O Bus Port. Again, two separate ports are needed for this function as well.

As a result of the above, it is clear that Minami does not have a "single read/write port" as recited in Applicants' independent claim 13, and instead teaches the need for at least two separate ports (the System Bus Port and the I/O Bus Port) and therefore cannot anticipate or render obvious this structure.

Moreover, as noted above, the claim requires that the single read/write port include a read channel and a write channel. At best, Minami's DMA controller is required to have two "read/write ports," one to the system bus and one to the I/O bus.

Even more importantly, Minami specifically teaches that these ports cannot operate independently and indeed specifically teaches that when one cannot operate independently as read and write channels. When one port is operating as a read channel, it cannot also operate as a write channel and vice versa. Confirmation of this conclusion is set out in section 8 on page 5 of the Official Action, towards the end of the bold portion of the Examiner's text. The Examiner quotes column 3, lines 25-32 of Minami as stating that it has a transfer rate of "(I/O bus width) x (system clock signal frequency) x ½" (Minami, column 3, lines 31-32). The use of ½ makes it clear that **either** a read function **or** a write function is being performed by Minami at any one point in time and therefore both cannot be performed at the same time **independently** of each other. If they could operate independently of each other, then there would be no need for the "1/2" factor reducing the "transfer rate".

Thus, not only does Minami fail to teach **a single read/write port**, but he fails to teach one in which the read and write channel can operate to "perform data reads and writes **independently** of each other." (emphasis added).

As this feature is present both in Applicants' independent apparatus claim 13 and independent method claim 28, and because these aspects are absent from the Minami reference, there is simply no support for any anticipation of claims 13 and 28 or claims 14-16 and 29-31 dependent thereon, respectively, and any further rejection thereunder is respectfully traversed.

In section 8 of the outstanding Official Action, in the second line on page 6, the Examiner points out that Minami discloses in Figure 2 a control line for carrying control signals. Figure 2 is also different from Applicants' invention in that it shows a "fly by" DMA which is described in the prior art portion of Applicants' specification with respect to Figure 1. In such prior art systems, only the **control** information passes through the DMA controller and **not the data** being transferred.

It is noted that independent claims 13 and 28 recite that the single read/write port is a read channel "operable to receive **data**" (emphasis added) from the data source and a write channel "operable to output said received **data**" (emphasis added) to a data destination. As is clearly known by those of ordinary skill in the art, control signals, as disclosed in Minami's Figure 2, are not "data" and therefore Minami's Figure 2 contains no disclosure of the invention in Applicants' independent claims 13 and 28 or claims dependent thereon.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 13 and 28 are generic to Applicants' claimed apparatus and method and these claims, and all claims dependent thereon, are clearly patentable over the only

cited reference and notice to this effect is respectfully requested. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of these claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100